A New Screening Method for Alleviating Transient Current Imbalance of Paralleled SiC MOSFETs

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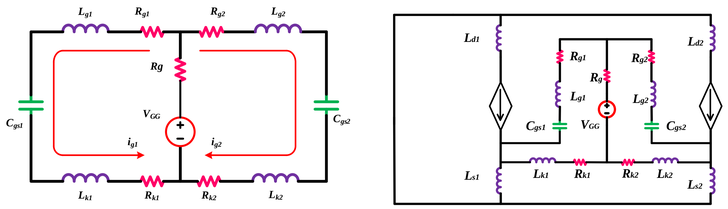
1 Motivation

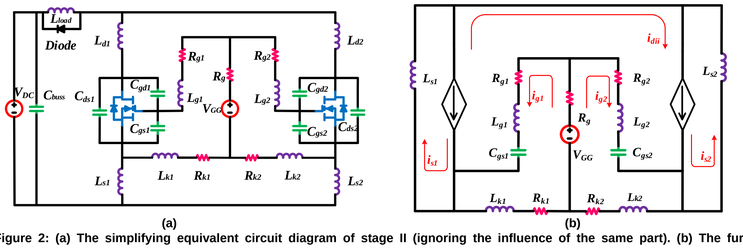
Due to material defects and immature process technology, the current level of SiC MOSFET is significantly lower than that of Si IGBT. Connecting multiple chips in parallel has become a common method to increase the current level. The existing chip classification principles are based on the premise that the module or circuit layout is completely symmetrical. However, in practice, it is very difficult for the layout to achieve complete symmetrical parallel branches, especially when many chips are connected in parallel. A chip screening method considering the influence of mismatched parasitic inductance induced by asymmetric layout of each chips is needed

2 Transient Current Sharing Model



(a) (b)

Figure 1: (a)The equivalent circuit diagram of stage I (V_{gs}<V_{th}). (b) The equivalent circuit diagram of stage II (V_{gs}>V_{th}) .



(a)

(b)

Figure 2: (a) The simplifying equivalent circuit diagram of stage II (ignoring the influence of the same part). (b) The further simplifying equivalent circuit diagram of stage II (ignoring the influence of the drain parasitic impedance).

TABLE I: Initial Calculation Parameters

Component	Parameter	Value	Parameter	Value
System Configuration	V_{dc}	600V	I_{load}	60A
Circuit Configuration	L_{d1}, L_{d2}	35nH	L_{s1}, L_{s2}	50nH
	L_{g1}, L_{g2}	15nH	L_{k1}, L_{k2}	20nH
SiC MOSFET (C3M0065100K)	C_{gs}	1388pF	V_{th}	4.103V
	C_{gd}	2pF	g	0.418A/V^2
	C_{ds}	56pF		
Gate Driver	V_{high}	15V	R_g	5Ω
	V_{low}	-5V	R_{g1}, R_{g2}	5Ω

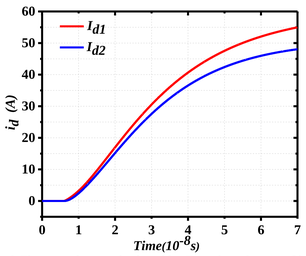
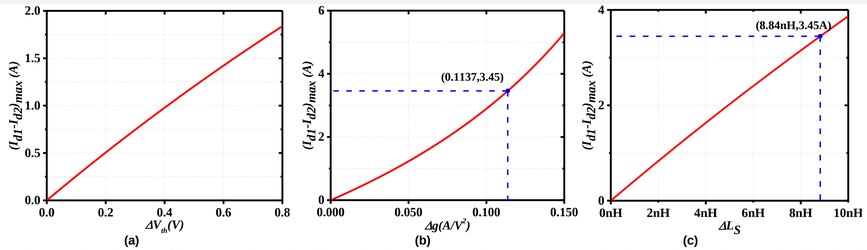
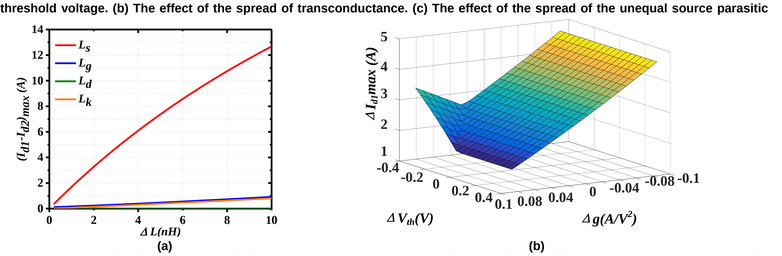


Figure 3:The waveform calculated by Transient Current Sharing Model



(a) (b) (c)

Figure 4:The influence of the main factors calculated by the transient current sharing model on the transient current sharing. (a) The effect of the spread of threshold voltage. (b) The effect of the spread of transconductance. (c) The effect of the spread of the unequal source parasitic inductance



(a) (b)

Figure 5: (a) The effect of the spread of layout parasitic inductance on the transient current sharing calculated by transient current sharing model. (b) The combined effect of threshold voltage and transconductance on transient current sharing calculated by transient current sharing model.

3 Chips Classification

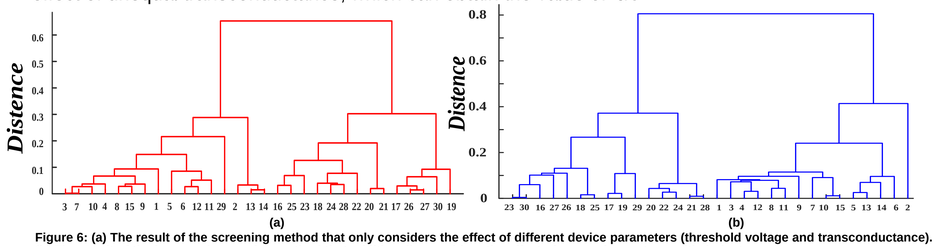
The screening method is based on the hierarchical clustering algorithm. The objective function of the screening method that only considers the effect of device parameters (the threshold voltage and transconductance) is as follows:

$$D_{ij} = \sqrt{(g_i - g_j)^2 + (V_{thi} - V_{thj})^2}$$

The improved objective function which additionally considers the effect of unequal layout parasitic inductance is as follows:

$$D_{ij} = \sqrt{[(g_i - g_j) - a]^2 + (V_{thi} - V_{thj})^2}$$

Figure 4 (b) and (c) are used to convert the effect of unequal source parasitic inductance into the effect of unequal transconductance, which can obtain the value of ‘a’.



(a) (b)

Figure 6: (a) The result of the screening method that only considers the effect of different device parameters (threshold voltage and transconductance). (b) The result of the improved screening method that additionally considers the effect of unequal layout parasitic inductance.

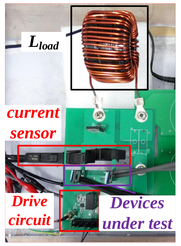
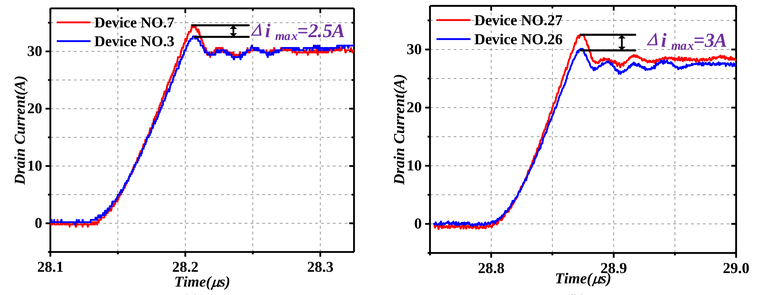


Figure 7: Double pulse experiment platform

TABLE II: Parasitic Inductance Extraction of Experimental Circuit by Q3D

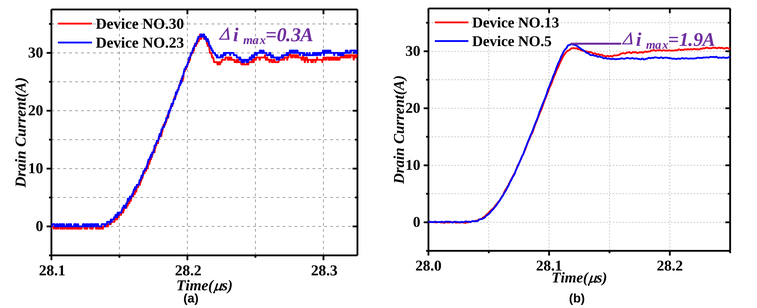
Circuit Configuration	Parameter	Circuit Configuration	Parameter
L_{d1}	37.32 nH	L_{k1}	20.03 nH
L_{d2}	36.83 nH	L_{k2}	19.92 nH
L_{s1}	60.02 nH	L_{g1}	15.08 nH
L_{s2}	51.62 nH	L_{g2}	15.53 nH

4 Experimental Results



(a) (b)

Figure 8: Experimental waveforms of parallel devices screened out by ordinary screening method (a) Turn-on waveform of device NO.3 and NO.7. (b) Turn-on waveform of device NO.26 and NO.27.



(a) (b)

Figure 9: Experimental waveforms of parallel devices screened out by improved screening method (a) Turn-on waveform of device NO.30 and NO.23. (b) Turn-on waveform of device NO.13 and NO.5.

TABLE III: THE MAXIMUM UNBALANCED CURRENT OF THE OTHER GROUPS OF CHIPS SELECTED BY THE TWO CLASSIFICATION METHODS

The results of the experiment selected by hierarchical clustering based on the threshold and transconductance		
DUT1	DUT2	$(I_{d1}-I_{d2})_{max}$
NO.3	NO.7	2.4A
NO.26	NO.27	2.93A
NO.8	NO.15	3.4A
NO.16	NO.25	2.6A
The results of the experiment selected by hierarchical clustering algorithm introducing loop mismatch		
DUT1	DUT2	$(I_{d1}-I_{d2})_{max}$
NO.30	NO.23	0.4A
NO.13	NO.5	1.9A
NO.19	NO.17	2A
NO.22	NO.24	1A

5 Conclusion

This paper proposes a new chip screening method based on hierarchical clustering algorithm. This screening method considers not only the effects of threshold voltage and transconductance but also the effects of asymmetry layout. And it can solve the unbalanced current caused by parasitic inductance mismatch. Experimental results show that the chip screening method which takes account of the influence of asymmetric layout is significantly better than the screening method that only considers the influence of the intrinsic parameters of the device.